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Ersin Bahceci,[1] Brian Enders,[2] Zain Yamani,[3] Serekbol Tokmoldin,[4] Aman Taukenov,[5] Laila Abuhassan,[6] and Munir Nayfeh[2,a)]

AFFILIATIONS

[1] Department of Metallurgical and Materials Engineering, Iskenderun Technical University, 31200 Hatay, Turkey
[2] Department of Physics, University of Illinois at Urbana-Champaign, 1110 W. Green Street, Urbana, Illinois 61801, USA
[3] Department of Physics, King Fahd University, Dhahran 34463, Saudi Arabia
[4] Institute of Physics and Technology, 050000 Almaty, Kazakhstan
[5] LED Systems Media, 050000 Almaty, Kazakhstan
[6] Department of Physics, University of Jordan, 19628 Amman, Jordan

[a)] **Corresponding author:** m-nayfeh@illinois.edu

ABSTRACT

We use silicon having multiple crystalline orientation domains and high metal doping in metal assisted chemical etching (MACEtch) in HF/H_2O_2. In device-quality silicon, MACEtch produces high-aspect ratio anisotropic (1-D) structures (wires, columns, pores or holes) and to a lesser degree non-high-aspect ratio luminescent (0-D) nano structures. While the 1-D structure symmetry is understood in terms of crystallography axis-dependent etching, predominantly along the <100> direction, the isotropic 0-D spherical symmetry etching is not understood. We observe in silicon having multiple crystalline orientation domains formation of metal tips (needles or whiskers) of diameters as small as 2-3 nm that bridge the metal to silicon and cause AFM/STM-like nanofabrication, producing 0-D mounds, indentations, or clusters. The formation of sharp needles can be understood in terms of charge injection/electric breakdown between metal clusters and silicon due to charge build-up. Silicon with high degree of impurities as well as with multiple crystalline orientation domains allow imaging these effects using electron spectroscopy without cross sectional cuts.

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I. INTRODUCTION

Metal assisted chemical etching is a wet anisotropic etching procedure for etching semiconductors[1,2] with a variety of applications.[3,4] One interesting procedure is etching silicon in an HF/H_2O_2 solution.[5,6] The procedure provides an etching rate that is highly dependent on the crystallographic directions, being fastest along the <100> Si direction (in the plane perpendicular to this axis) and slowest along the <111> Si direction, making it the stopper direction. Metal ions assisted chemical etching of silicon (Ag^{3+}/HF) has also proved to be anisotropic along the <100> Si axis.[7–9] The large variance in etching rates in HF/H_2O_2 (a factor of ~ 100) enables synthesis of high aspect ratio (1-D) structures, such as wires, columns, pores or holes with lengths in the micrometer scale regime, with a wide range of high tech applications. The role of the metal, which is typically a noble metal, is oxidation-based generation and injection of charge into silicon, which speeds up the otherwise slow etching in HF/H_2O_2.

Recent developments have shown that in addition to the 1D structures (Li) the procedure simultaneously produces highly interesting non-high aspect ratio structures, such as (0-D) nano particles,[6] pointing to effects in which there is simultaneous cylindrical and spherical symmetry etching processes. Though the mechanism of formation of the 1-D structures are well understood in terms of crystallography axis-dependent etching, namely along the <100> direction, the mechanism of formation of the finer 0-D structures are not understood. Etching is not crystal- orientation dependent that enables anisotropic etching; rather it occurs

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isotopically, proceeding equally in vertical (depth) and lateral directions.

In this paper we conduct experiments on metal assisted chemical etching in HF/H_2O_2 of silicon with high degree of impurities as well as with multiple crystalline orientation domains. Multiple crystalline orientations facilitate imaging, revealing internal etching effects using electron spectroscopy without cross sectional cuts, which makes it more straightforward to discern the interplay/interdependence between the two etching symmetries: anisotropic high-aspect ratio (1-D) (resulting in wires, columns, pores or holes) and the non-high-aspect ratio (0-D) (resulting in nano structures). The interface between silicon and the metal is closely examined to study the effect of charge accumulation and injection from the metal to Si on synthesis of various dimensionality structures. Our measurements indicate that in addition to the fact that charging of silicon activates the otherwise weak crystollagraphical dependent etching it causes production of sub 3-nm diameter sharp tips/needles, causing isotropic STM/AFM-like 0-D nanofabrication.

II. EXPERIMENTAL

The silicon wafers used in the present measurements have multiple crystalline orientation domains, and high metal levels; those silicon wafers come from a metrological process (developed at the Institute of Physics and Technology (IPT), Kazakhstan (IPT process).[10] In the IPT silicon manufacturing process, poly- and mono-crystalline p-type silicon, with resistivity of 0.24 Ohm-cm and unpolished wafers are grown by the Czochralski method and short of the expensive purification step of chlorosilane processing. This process constitutes a metallurgical refining lower-cost, short-cut technology for production of silicon. The wafers were characterized for solar cell applications (solar grade silicon) at the US National Renewable Energy Laboratory (NREL) and the Solar Power Industries (SPI).[11] The tests showed that not only the characteristics of IPT wafers, namely the distribution of the domains of crystal axes, and the degree of impurities (conductivity or resistivity) differ over wide ranges from wafer to wafer, they also vary from region to region on the same wafer. Tests showed metal levels of ~ 1 ppbmwt, which is suitable for poor solar grade silicon applications. However, measurement of boron (B) and phosphor (P) showed high levels. For instance, it found the boron, aluminum (Al) and phosphor levels at 7.7 - 24 ppmwt, 1.8 - 22 ppmwt, and 1.3 - 44 ppmwt respectively. Resistivity measurements of the wafers gave 0.1 to 0.3 Ω-cm, with a corresponding lifetime of charge carriers of 0.1 - 0.3 μs. Those values are outside the SPI's minimum requirement of (worse than) Upgraded Metallurgical Grade Silicon for photovoltaic device operation, which is Boron < 0.5 ppmwt, Phosphorus < 2.0 ppmwt. It is to be noted that silicon wafers or wafer strips (pieces) used in this work refer to IPT wafers unless, for the purpose of comparison, they are designated as device quality electronic grade (EGSi).

We start out by wafer strips/pieces of ~ 14mm × 30mm rectangles cut out from a number of silicon wafers for easy handling; and sonicate the wafer strips in acetone for five minutes and then rinse them in water and isopropyl alcohol. The strips are immersed in a bath, which is a 3:1 mixture of hexachloroplatinic acid and HF for about 10 minutes to deposit platinum on the surface via a spontaneous electrochemical reaction, which reduces the platinic acid to platinum. We then remove/separate the wafers from the bath, followed by rinsing with isopropyl alcohol and drying by a nitrogen gas jet. The strips are then immersed in an etching bath, individually or in a stack formation with a certain interspacing. The chemical etchant is a solution of hydrogen fluoride acid, methanol, and hydrogen peroxide ($HF:CH_3OH:H_2O_2$) of 1:2:3 ratio by volume of standard commercially available concentrations (while the methanol can be purchased pure, non-fuming aqueous HF has a standard concentration of 49% HF, and hydrogen peroxide is an aqueous solution of 30% H_2O_2).[6]

The materials and structures are characterized using several procedures including scanning electron microscopy (SEM), X-ray photoelectron spectroscopy, and imaging and material analysis mapping using energy-dispersive X-ray spectroscopy (EDX), while the optical properties are characterized using photoluminescence spectroscopy, fluorescence microscopy. The visible luminescence of the wafers is monitored at all stages/steps of the process: before and after platinum deposition step, after etching step, after sonication step, and after recovery of luminescent Si nanoparticles in a colloid solution. To obtain the luminescence spectra, we excite using 365, 300- or 254-nm incoherent light. For detection, we use a fiberoptic spectrometer that uses optical fibers to extract the emission. We use a near-infrared holographic grating with groove density of 600/mm with a blaze wavelength of 0.4 μm and with best efficiency in the range 0.25–0.80 μm.

III. MEASUREMENTS

The IPT Si strips are immersed for about 10 minutes in a bath, which is a 3:1 mixture of hexachloroplatinic acid and HF. Figure 1a shows a scanning electron microscope image taken from platinum deposited the wafer. It first shows the high roughness of the crystal. Second, it shows formation of Pt nanoparticles, which indicates that despite the high roughness of the crystals, surface diffusion of platinum atoms is sufficiently high (weak metal-Si bond) to allow formation of nanoparticles. Material analysis using energy-dispersive X-ray spectroscopy (EDX) provides elemental analysis or chemical characterization of the sample. EDX spectra were taken from four areas on this sample (labeled 1, 2, 3, and 4) with incident 30 KV x-ray. The atomic percentage over the entire cluster labelled 4 are: 11.5, 4.4, 76.5, and 6% for carbon, oxygen, silicon and platinum respectively. The atomic percentages over the entire cluster labeled 2 are: 6.4, 3.2, 82.3, and 6.3% for carbon, oxygen, silicon and platinum respectively. Analysis of spots 1 and 3 showed no platinum as shown in Figure 1b. After depositing platinum on several wafer pieces, we removed the wafers from the bath, rinsed them with isopropyl alcohol, and dried them by a nitrogen gas jet. At this stage (right after Pt deposition step), exposing the wafer pieces to UV show that they are not luminescent. Moreover, sonication of such wafers do not result in a luminescent material. This indicates that no sharp structuring of Si particles had occurred at this stage.

The wafers are then immersed individually or in a stack formation with a certain interspacing in an etching bath.[6] Figure 2a–b show SEM images of some sections of the etched wafers. It shows that, on some sections of the wafer, etching is lateral (sliding on the surface), making shallow grooves. This is consistent with the fact that that etching has a preferred direction, and that the IPT wafer may

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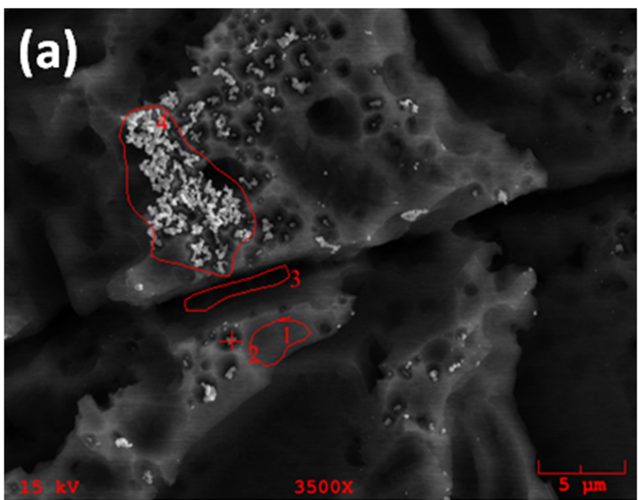

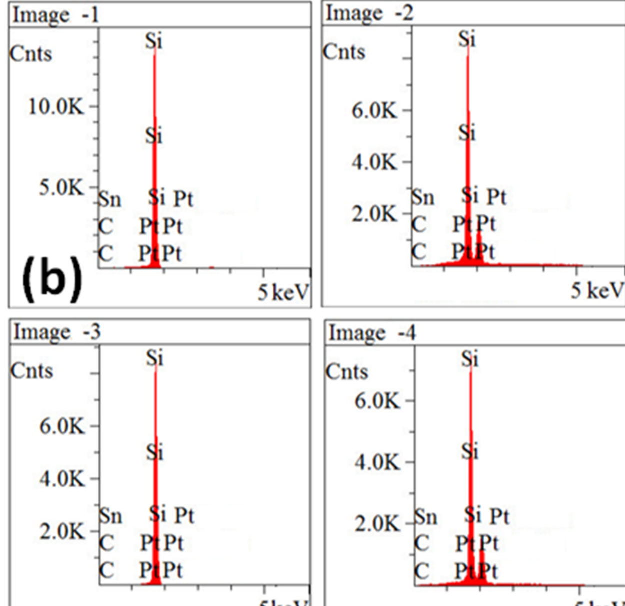

FIG. 1. (a) SEM image of platinum chemical deposition on IPT silicon. Deposition on wafer shows formation of Pt nanoparticles. (b) Material analysis using energy-dispersive X-ray spectroscopy (EDX) of four regions labeled from 1 to 4 on (a) provides elemental analysis or chemical characterization of the sample. It plots the number of counts (Cnts) as a function of electron energy in KeV.

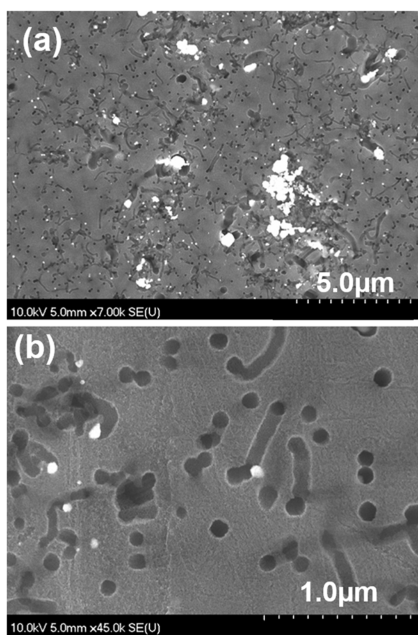

FIG. 2. SEM images of the surface of IPT silicon wafers after platinum deposition and etching. (a) Etched wafers, showing etching, in some regions, is lateral (sliding on the surface), making shallow grooves while others are normal to the surface. (b) High-resolution imaging of another section of the wafer.

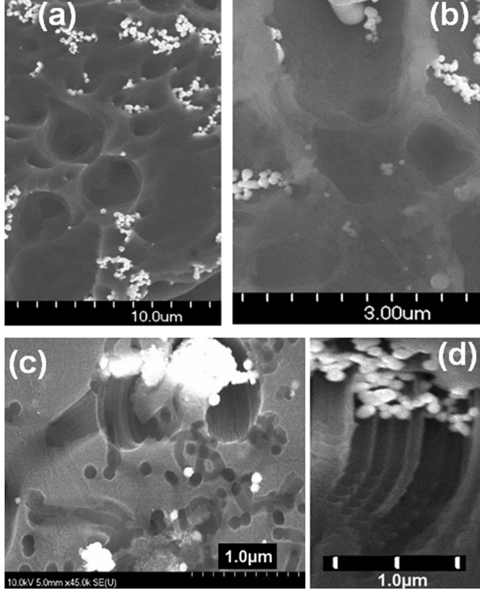

FIG. 3. Etched wafers. (a-b) show some particles moving in side pockets indicating horizontal <100> direction. (c-d) Platinum clusters move together in the etching process, making individual grooves, suggesting electrical interconnection between those individual platinum nanoparticles.

not have the same <100> crystal plane orientation over the entire wafer as found in a single crystal high- or device-quality Si wafers (electronic grade Si wafers (EGSi)). In fact, for a <100> EGSi wafers platinum burrows and etches upright perpendicular to the surface of the crystal.

Figure 3a–b show that particles are moving in side pockets in IPT wafers, indicating horizontal <100> directions in these pockets. Figure 3c–d show that nanoparticles in some clusters move together during etching, while making individual grooves,

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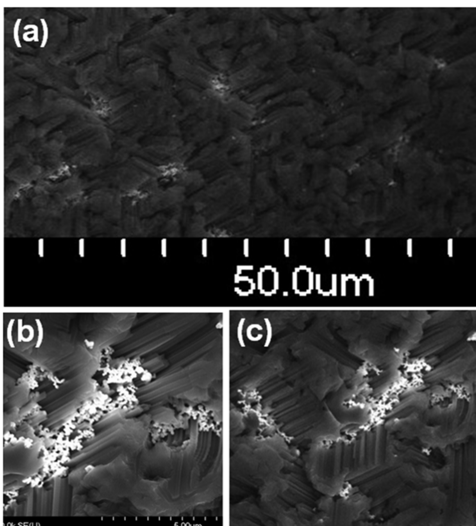


FIG. 4. (a, b-c) SEM of etched IPT silicon wafer. Pores opened up exposing interior etching tracks of the platinum nano particles in a variety of directions, without taking cross-sectional cuts, indicating multiple crystalline orientation domains.

suggesting electrical interconnection between those individual platinum nanoparticles.

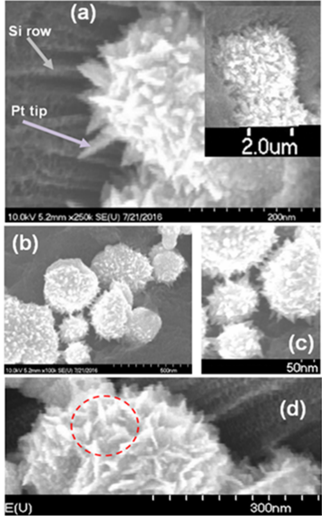
Upon inspection of etched samples with SEM, as shown in the three images in Figure 4a–c, we can observe the interior etching tracks of the platinum nano particles as they are exposed. Thus, interior etching of the wafer can be accessed using SEM imaging without taking cross-sectional cuts. The pores or tracks appear in a variety of directions, indicating multiple crystalline orientation domains. The reduced mechanical strength may be related to the multiple crystalline orientation domains as well as to the strong strain resulting from etching.

Figure 5a presents an image of a Pt nanoparticle cluster from the side vantage of a pore (side view) at a point during etching. It shows very sharp tips protruding out from a Pt cluster, bridging it to the silicon material. Figure 5a (inset) shows the same effect from the top view vantage of a Pt cluster sinking down into the silicon substrate. Figure 5b–c show similar sharp tips forming between neighboring platinum clusters, which bridge and essentially "electrically connect" them such that they move in concert in the etching process.

Figure 5d show that tips come in the shape of bipyramids, which are characteristic of gold, silver, or platinum growth.[12,13] Those have two sharp tips at opposite ends which defines the length (typically 50-60nm), with the thickest dimension (typically 15-20nm) being at the waist. The radius of curvature of the tips are as small as 1-2nm. Figure 5d also labels typical tips. Figure 5e and its inset show the various dimensionality structures made in the MACEtch produces. We labeled the anisotropic 1-D structures of wires or columns, and pores and grooves, as well as the non-high-aspect ratio luminescent 0-D nano structures.

In MACEtch,[5] Li and Bohn postulated that platinum nanoparticles on the surface act as a local cathode that mediates the reduction of H_2O_2, producing holes in the etchant. When charge accumulates in the Pt nanoparticles, charge breakdown accompanied with a current surge could take place laterally, across the liquid and the Pt-Si interface/Schotcky potential barrier. The Pt-Si interface (contact point), acts as the local anode. The current surge softens or even melts the nano platinum, creating lateral conducting dissipation paths as in electric percolation. Electrical breakdown or dielectric breakdown proceeds when current flows through an electrical insulator, resulting from an applied voltage across it that exceeds the breakdown voltage. This results in the insulator becoming electrically conductive.

We believe that the electric breakdown between the platinum clusters as well as between platinum and silicon contributes to the grown of the platinum sharp probes. The current surge softens and reforms the platinum nanoparticles, assisting the growth of the very sharp tips. Note that voltage break down has been used to



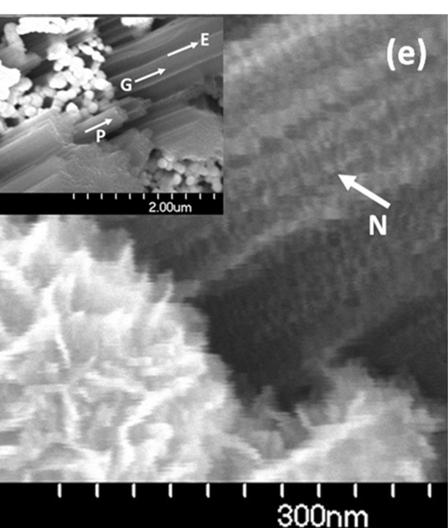


FIG. 5. SEM of Pt nanoparticles after etching (a) Pt nanoparticle cluster from the side vantage of a pore (side view) at a stage after etching. It shows very sharp tips protruding out from Pt, bridging the nanoparticle to the silicon material. (inset) Top view vantage of a Pt nanoparticle cluster sinking down into the silicon substrate. (b-c) Sharp tips forming between neighboring platinum clusters (d) tips have bipyramids shapes characteristic of gold, silver, or platinum growth (e) and inset label examples of 1-D structures: pores (P), grooves (G), edges (E), and nanostructures (N).

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sharpen metal tips especially those used in STM for imaging and nanofabrication. In the procedure, the tungsten tip is first moved away from the silicon substrate, followed by applying across a large voltage pulse of ~ 100 V, which produces a field-emission current between the tip and the surface. This tends to anneal and sharpen the tip. Such action sharpens the tip but sometimes produces a multiple whiskers on the tip. Imaging using those produces doublets or triplets depending on the number of whiskers.[14] Thus, in this process, metal structures generate as well as inject charge across the metal-silicon interface, which enhances the chemical etching of silicon in wet HF for example.

As the platinum cluster etches and sinks into the silicon wafers by dissolution of the charged silicon by the HF/H_2O_2 the multiple tips or needles plow into silicon to create the fine structures on the sidewalls of the pores as can be seen in the figure. Such sharp tips are expected to produce very strong local electric field, which facilitates dielectric breakdown and concentration of the accompanying current surge hence surface modification at the nanoscale resolution. The process mimics the use of an STM tip or a conductive AFM tip in nanolithography in the presence of HF.[15–17]

The breakdown threshold is estimated from the dielectric strength of the etching solution HF/H_2O_2 in water. The dielectric strength of distilled water is 65 - 70 MV/m.[18] Because of the presence of the acid and oxidizer in the water and the presence of contain minute defects or particles, the practical dielectric strength will be a fraction of the intrinsic dielectric strength of an ideal, defect-free, material (~5 MV/m). Moreover, very thin layers (<100 nm) become partially conductive because of electron tunneling. For a conducting sphere of radius 175nm, a voltage of 0.85 V is needed to reach this field on the surface. This corresponds to charging the sphere with a total of ~ 200 hole charges.

The rows made by the tips are actually spotty rather than continuous. The spot on the average is 3-6 nm across as can be seen in Figures 6. This is similar to nanofabrication using an STM operating in the field emission mode.[19]

Figure 7a presents the photo of processed strips (after Pt deposition and etching) under irradiation with UV radiation at a wavelength of 365 nm, showing orange/red luminescence. The red luminescence confirms that at this stage sharp structuring of Si particles

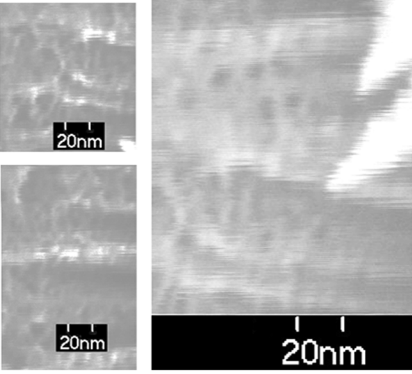

FIG. 6. Four examples of SEM images of the inner sidewalls of pores. The rows are actually spotty not continuous. The spots are the average 3-6 nm across.

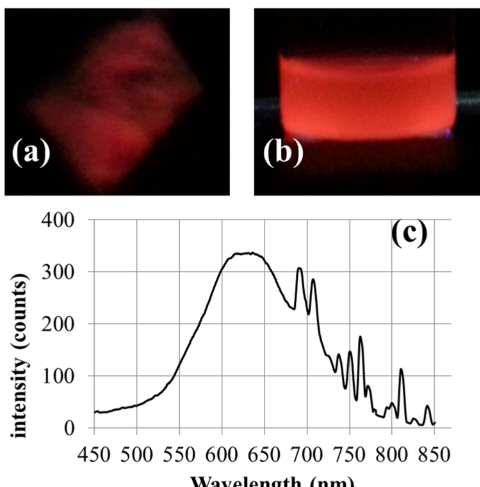

FIG. 7. Luminescence of silicon, after Pt deposition and etching, under irradiation with UV radiation at a wavelength of 365 nm (a) photo of processed wafers (b) photo of Si nanoparticle liquid colloid after nanoparticle dislodge and recovery using ultrasound treatment (c) luminescence spectrum of the nanoparticle colloid. The sharp peaks on the red wing of the bands are residual structure from increased scattering of the lamp light.

had taken place. The wafer strips or pieces are then placed in a solvent of choice (isopropanol alcohol), and sonicated for 5 minutes. The process dislodges some of the ultrafine structures (0-D Si nanoparticles) in the liquid. The nanoparticle concentration can be enriched, if desired, by using larger or multiple wafers or by recycling the wafer. The enriched nanoparticle colloid is then centrifuged to filter out larger chip pieces that may have broken off due to the fragility of the wafer, leaving behind a stable colloid. In room light, the colloid is clear and transparent. Under UV irradiation, the colloid is red luminescent as shown in Figure 7b. The corresponding luminescence spectrum of the colloid is given in Figure 7c. The spectrum is a band extending from 530 nm to 750 nm with sub structure at 590 and 650 nm. We attribute the red wing fine structure in Fig 7c to scattering by larger components present in the colloid such as the bi-pyramidal structures or/and larger Si pieces that break from the wafer upon sonication since IPT wafers are fragile due to the domain multiplicity of crystalline directions.

IV. ANALYSIS (HOLE SHIELDING BY IMPURITY)

The maximum impurity content of the purity of acceptable electronic grade is ~1 ppbw. Increased impurities, such as metal and boron and phosphor shorten charge carrier lifetime and compromises electronic device operation.[20] However, low cost solar cell devices with efficiency as high as 14 percent have been built from solar grade silicon (SoGSi) that is less pure (boron/phosphor) than the electronic grade, down to a limit on the maximum impurity content of ~1ppmw, nearly a factor of 1000.

In the IPT wafers metal levels of ~ 1 ppbmwt were found. Moreover, impurity measurement found the boron, aluminum (Al) and phosphor levels at 7.7-24 ppmwt, 1.8-22 ppmwt, and 1.3-44 ppmwt respectively.[11] Because the etching rate in this process depends on

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the hole density, having too high impurity content in the wafer may reduce the etching rate as impurities reduce the lifetime of the injected hole carrier. In fact, resistivity mapping of the wafers gave 0.1 to 0.3 Ω-cm, with a corresponding lifetime of charge carriers of 0.1 - 0.3 μs, much reduced from 220 us for single crystal silicon wafers. Having short carrier lifetime may compromise the yield or even interrupt the process since the etching process requires charging of silicon. It is plausible that the injected holes do not penetrate the silicon layer too deep (stay confined mostly to the surface), shielding the holes and resulting in much less interaction with bulk impurities. The diffusion length of the *minority* charge carriers L_{diff} which is related to τ_{bulk} by

$$L_{\text{diff}} = [D\,\tau_{\text{bulk}}]^{1/2} \tag{1}$$

$$D = \mu_{\text{drift}} kT/q \tag{2}$$

where q electrical charge, μ_q its electrical mobility is related to its generalized mobility μ by the equation $\mu=\mu_q/q$. The parameter μ_q is the ratio of the particle's terminal drift velocity to an applied electric field.[21,22]

For a wafer with standard mobility values, namely EGSi, the lifetime measured τ_{bulk} = 220 μs corresponds to L_{bulk}790 μm. For the IPT wafers used in this experiment, τ_{bulk} = 0.1 μs, which gives a much reduced L_{bulk} 16 μm, essentially confining the holes to the top skin of the wafer. This affords the process two advantages. First, concentration of holes in a sub layer of the wafer enhances the hole-charge density, which provides sufficiently high and aggressive HF-etching of silicon, condition favorable for efficient formation of silicon nanoparticles. Second, the etching process is mostly a surface etching process, bulk impurities do not factor very much. Figure 4d shows how the hole injection and etching is spatially localized near individual platinum nanoparticles. The effect of doping on the process was examined using device-quality electronic grade wafers (EGSi).[23–27] For low impurity doping densities (<< 10^{15}/cm^3 boron or very high resistivity), the injected holes penetrate very deep in the wafers, resulting in very low charging density, resulting in low etching rate causing charring of the wafers with no formation of Si nanoparticles. On the other hand, for very high level of impurity doping (>> 10^{15}/cm^3 boron or very high conductivity), the hole concentrates on the surface creating very high charge density and high etching rate causing polishing of the wafer with no formation of luminescent Si nanoparticles. A doping such that the resistivity falls in the range 4-8 Ω.cm^{-1} is optimal. The etching mechanism of the Pt catalyst is summarized as follows: peroxide dissociates on the surface of platinum particles, which oxidizes the surrounded silicon, and the oxide is, in turn, removed by hydrofluoric acid. This process allows the platinum particles to effectively 'eat' into silicon.

In fact, as the SPI tests of solar cells built from the IPT grade showed above short lifetime of holes implies that photo-produced electron – hole pairs (excitons) in the bulk of the wafer by impinging light are expected to recombine fast before they can be separated and transported across the silicon layer to the surface.

Exponentially growing demand for silicon has fueled extensive research and development to develop low-cost processes for single crystal, polycrystalline, nano clusters or film ribbon from starting materials that are inexpensive, without high-power processing demands. Among the applications that drive this demand ate electronics, optics, and renewable green energy harvest and storage, and lighting. Specific device applications include silicon solar and biofuel cells, super capacitors, nanophosphors for solid-state diode lighting, photo detectors, and supporting nano electronics.[23–27]

V. CONCLUSION

In conclusion, we examined the interplay of anisotropic 1-D cylindrical and isotropic 0-D spherical symmetry etching in metal assisted chemical etching of silicon with multiple crystalline orientations in HF/H_2O_2. While the 1-D symmetry is well understood in terms of crystallography axis-dependent etching, we show that isotropic 0-D spherical symmetry etching take place in terms of STM/AFM-like proximal probe nanofabrication. Multiple very sharp metal tips (bipyrmidoial) of diameters as small as 1-2 nm are produced via the charge injection/electric breakdown between metal clusters and silicon due to charge build-up in the metal. The results also demonstrate low-grade metallurgical silicon route using solar grade silicon (SoGSi) with high impurity, short carrier lifetimes, and multiple crystalline orientation domains produce high-quality red luminescent silicon nanoparticles, with efficient yield.

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